1. Architecture of 8051 Microcontroller

The various components of 8051 Microcontroller are as follows:

(i) CPU (Central Processing Unit):
- Composed of ALU, 16-bit Program Counter and Data Pointer, 8-bit Stack Pointer, Special Function or Special Purpose Registers.
- The ALU is composed of ALU, Accumulator, B-Register and two Temporary Registers and PSW (Program Status Word); The Accumulator serves as 8-bit source or destination register in case of DATA TRANSFER operations, source and destination register in case of ARITHMETIC, LOGICAL and DATA EXCHANGE and SWAP operations; The B-register serves as a source and destination register in case of MULTIPLICATION and DIVISION operations.
• The contents of Accumulator and B-register are applied to ALU through their respective temporary registers.

• The ALU can perform the following functions:
  ✓ Arithmetic Functions:
    o Bit level and Byte Level Addition Operation with and without carry
    o Bit level and Byte Level Subtraction Operation with borrow
    o 8-bit Multiplication and Division Operation
    o 8-bit Binary to BCD Conversion
  ✓ Logical Functions:
    o Bit level and Byte Level AND operation
    o Bit Level and Byte Level OR operation
    o Bit Level and Byte Level CLEAR operation
    o Bit Level and Byte Level NOT operation
    o Byte Level XOR operation
    o Byte Level ROTATE or SHIFT operations

• The PSW (Program Status Word) or Flag Register is a 7-bit register and indicates the status of accumulator after a ARITHMETIC or LOGICAL operation.

```
  7  6  5  4  3  2  1  0
 CY AC F0 RS1 RS0 OV — P
```

- CY[Carry or Borrow Bit] = 1 indicates a CARRY has occurred out of higher order nibble of accumulator or borrow has occurred into higher order nibble of accumulator.
- AC[Auxiliary Carry or Borrow Bit] = 1 indicates a CARRY has occurred out of lower order nibble of accumulator or borrow has occurred into lower order nibble of accumulator.
- F0 – General Purpose User Definable Flag
- RS1 , RS0 = Register Bank Select bits

```
  RS1 RS0
  0  0 Select register bank 0
  0  1 Select register bank 1
  1  0 Select register bank 2
  1  1 Select register bank 3
```

- OV[Overflow or Sign] bit = 1 , Indicates the result in the accumulator is a negative number in case of signed addition and the result has exceeded the capacity of accumulator in case of unsigned addition.
- P[Parity] bit = 1 , indicates the result in the accumulator has ODD PARITY.

• The 16-bit DPTR(DATA POINTER) is used to hold memory address for INTERNAL/EXTERNAL CODE ACCESS and EXTERNAL DATA ACCESS.

• The 16-bit Program Counter holds the address of NEXT INSTRUCTION to be executed stored in the INTERNAL ROM. The RESET value of PC is 0000H .It increments or decrements by:
  ✓ 1 for 1-BYTE INSTRUCTION
  ✓ 2 for 2-BYTE INSTRUCTION
  ✓ 3 for 3-BYTE INSTRUCTION

The 16-bit PC is used to hold memory address for INTERNAL/EXTERNAL CODE ACCESS.

• The 8-bit Stack Pointer holds the address of TOP of STACK present in the INTERNAL RAM. TOP of STACK is the STACK location where a byte has been lastly PUSHED into. The SP increments by 1 for every PUSH operation and decrements by 1 for every POP operation. The RESET value of SP is 07H.
INTERNAL or ON-CHIP RAM or DATA MEMORY:
- Consist of totally 256 memory locations; The lower 128 memory locations are called General Purpose Area and its split-up is as follows:
  - First 32 locations [00 to 1F] for Register Bank (Register are manipulated as BYTE)
  - Next 16 locations [20 to 2F] for BIT ADDRESSABILITY (Individual bits of a memory location can be manipulated)
  - Last 80 locations [30 to 7F] for SCRATCHPAD purpose during ARITHMETIC, LOGICAL and DATA TRANSFER, EXCHANGE operations.
- The location 08H to 7FH can also be used as LIFO STACK.
The upper 128 memory locations are called SPECIAL PURPOSE AREA and consist of registers associated with ALU, on-chip MEMORIES and PERIPHERALS.
The type of ON-CHIP RAM is SRAM [or Static RAM]

INTERNAL or ON-CHIP ROM or PROGRAM MEMORY or CODE MEMORY:
- Consist of totally 4K memory locations.
- Presence of on-chip ROM is optional; A ROMLESS variant of 8051 microcontroller is 8031 microcontroller.
- The type of ROM implemented in 8051 microcontroller can be any one of the following:
  - Masked ROM
  - OTP (One Time Programmable) ROM [also called as PROM]
  - UV-EPROM
- The programs stored in ROM are called FIRMWARE.

I/O PORTS:
- There are totally four 8-bit I/O Ports namely PORT 0, PORT 1, PORT 2, PORT 3.
- Three out of four ports namely PORT 0, 2 and 3 are multifunctional PORTS.
- Two types of operating modes of 8051 microcontroller with respect to its ports are:
  - (i) SINGLE CHIP MODE
  - (ii) EXPANDED MODE.
- In SINGLE CHIP MODE, all the software and data are internally embedded into the MICROCONTROLLER and external memory chips are not used. In this mode all the four ports behave as GENERAL PURPOSE I/O ports.
- In EXPANDED MODE, the software and data that are more than the CAPACITY of ON-CHIP MEMORIES are stored in OFF-CHIP MEMORIES and external devices are interfaced to MICROCONTROLLER. In this mode the PORTS behave as follows:
  - PORT 0 serves as LOWER ORDER MULTIPLEXED ADDRESS/DATA BUS (AD7-AD0)
  - PORT 2 serves as HIGHER ORDER ADDRESS BUS (A15-A8)
  - PORT 3 serves for (i) SERIAL DATA COMMUNICATION (ii) EXTERNAL MEMORY READ and WRITE operations (iii) EXTERNAL LEVEL or EDGE TRIGGERED GENERAL PURPOSE INTERRUPTS (iv) TWO CLOCK PULSE inputs for operating INTERNAL TIMERS as COUNTERS.
  - PORT 1 serves as GENERAL PURPOSE BIDIRECTIONAL I/O PORTS.
- The SFRs associated with I/O Ports have the same name as their Ports. The individual bits of each port can be manipulated.

TIMER/COUNTER:
- There are totally two 16-bit timers namely TIMER 0 and TIMER 1 in 8051 microcontroller and three timers namely TIMER 0, 1 and 2 in 8052 microcontroller.
- The TIMER can function as both timer as well as counter. When operating as timer, it receives the clock pulses from the INTERNAL OSCILLATOR. When operating as counter, it receives the clock pulses from the TIMER pins of PORT 3.
- The TIMER/COUNTER module operates in the following four modes:
- 13-bit TIMER or COUNTER [MODE 0]
- 16-bit TIMER or COUNTER [MODE 1]
- 8-bit TIMER or COUNTER with AUTO-RELOAD FEATURE [MODE 2]
- 8-bit TIMER or COUNTER without AUTO-RELOAD FEATURE [MODE 3]
- The overflow of the TIMER or COUNTER is incremented by means of their RESPECTIVE TIMER OVERFLOW INDICATION FLAGS.
- The SFRs associated with TIMER/COUNTER module is TMOD (TIMER/COUNTER OPERATING MODE SELECTION REGISTER) and TCON (TIMER/COUNTER OPERATION CONTROL REGISTER), HIGHER and LOWER order bytes of INDIVIDUAL TIMER/COUNTERS.

SERIAL COMMUNICATION PORT:
- The SERIAL PORT of 8051 microcontroller supports FULL DUPLEX COMMUNICATION (i.e.) it can SIMULTANEOUSLY TRANSMIT or RECEIVE DATA from an EXTERNAL DEVICE.
- The SERIAL PORT operates in the following four operating modes:
  - 8-bit TRANSMISSION/RECEPTION [MODE 0]
  - 10-bit TRANSMISSION/RECEPTION [MODE 1]
  - 11-bit TRANSMISSION/RECEPTION [MODE 2]
  - 11-bit TRANSMISSION/RECEPTION [MODE 3]
- In MODE 0 and 2, the baud rate of serial communication is fixed. In MODE 1 and 3, the baud rate of serial communication is variable and depends on the value loaded in TIMER 1 [TH1].
- BAUD RATE of SERIAL COMMUNICATION is the number of SIGNAL CHANGES occurring per second. SIGNAL is change in VOLTAGE or FREQUENCY or PHASE.
- The SFRs associated with SERIAL PORT are SCON (SERIAL DATA COMMUNICATION CONTROL REGISTER), PCON (POWER MODE CONTROL REGISTER), SBUF (SERIAL BUFFER, combination of TRANSMIT BUFFER and RECEIVE BUFFER)

INTERRUPT:
- 8051 Microcontroller supports 5 hardware interrupts. They are (i) 2 GENERAL PURPOSE EDGE or LEVEL TRIGGERED INTERRUPTS (ii) 2 TIMER/COUNTER OVERFLOW INDICATION INTERRUPTS (iii) 1 SERIAL COMMUNICATION COMPLETION INDICATION INTERRUPT
- The SERIAL COMMUNICATION COMPLETION INDICATION INTERRUPT is obtained by the LOGICAL OR of TRANSMISSION COMPLETE interrupt and RECEPTION COMPLETE interrupt
- All the interrupts are VECTORED INTERRUPTS (i.e.) The INTERRUPT VECTOR ADDRESS of these interrupts are PREDEFINED, INTERRUPT VECTOR ADDRESS is the STARTING ADDRESS of a INTERRUPT SERVICE ROUTINE.
- The SFRs associated with interrupts of 8051 microcontroller are INTERRUPT ENABLE/DISABLE REGISTER, INTERRUPT PRIORITY CONTROL REGISTER.
- The priority of the interrupts are as follows:

<table>
<thead>
<tr>
<th>Interrupt Source</th>
<th>Vector Address</th>
<th>Priority within Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>External Interrupt 0</td>
<td>0003H</td>
<td>Highest</td>
</tr>
<tr>
<td>Timer 0 Interrupt</td>
<td>000BH</td>
<td>Highest</td>
</tr>
<tr>
<td>External Interrupt 1</td>
<td>0013H</td>
<td>Highest</td>
</tr>
<tr>
<td>Timer 1 Interrupt</td>
<td>001BH</td>
<td>Highest</td>
</tr>
<tr>
<td>Serial Port Interrupt</td>
<td>0023H</td>
<td>Lowest</td>
</tr>
</tbody>
</table>
TIMING and CONTROL CIRCUITRY:
- The TIMING and CONTROL circuitry is used for GENERATING TIMING, CONTROL and STATUS signals that is required for operation of INTERNAL and EXTERNAL CIRCUITRIES of 8051 microcontroller IN SYNCHRONISM.

### 2. Pin Diagram of 8051 Microcontroller

<table>
<thead>
<tr>
<th>PIN NO.</th>
<th>PIN or SIGNAL NAME</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>40</td>
<td>VCC</td>
<td>SUPPLY VOLTAGE</td>
</tr>
<tr>
<td>20</td>
<td>VSS</td>
<td>GROUND</td>
</tr>
<tr>
<td>1-8</td>
<td>P1.0 – P1.7</td>
<td>8-bit Bidirectional I/O port in SINGLE CHIP MODE and EXPANDED mode. Receives A0-A7 during program verification of ROM. When a pin has 1 in it, it acts INPUT PIN. When a pin has 0 in it, it acts as OUTPUT PIN. Has Internal PULL-UP RESISTORS.</td>
</tr>
<tr>
<td>39-32</td>
<td>P0.0 – P0.7</td>
<td>8-bit Bidirectional I/O port in SINGLE CHIP MODE. Serves as LOWER ORDER MULTIPLEXED ADDRESS and DATA BUS (AD7-AD0) in EXPANDED MODE. Uses INTERNAL PULL-UP RESISTORS in this case. Transmits CODE BYTES during program verification of ROM. Uses EXTERNAL PULL-UP RESISTORS in this case. When a pin has 1 in it, it acts INPUT PIN. When a pin has 0 in it, it acts as OUTPUT PIN.</td>
</tr>
<tr>
<td>28-21</td>
<td>P2.7 – P20.0</td>
<td>8-bit Bidirectional I/O port in SINGLE CHIP MODE. Serves as HIGHER ORDER ADDRESS BUS (A15-A8) in EXPANDED MODE. When a pin has 1 in it, it acts INPUT PIN. When a pin has 0 in it, it acts as OUTPUT PIN.</td>
</tr>
<tr>
<td>10-17</td>
<td>P3.0 – P3.7</td>
<td>8-bit Bidirectional I/O port in SINGLE CHIP MODE. When a pin has 1 in it, it acts INPUT PIN. When a pin has 0 in it, it acts as OUTPUT PIN. Has Internal PULL-UP RESISTORS. Special purpose I/O pins in EXPANDED MODE. P3.0 (RxD) – Serial Input Port (Connected to SERIAL RECEIVE BUFFER) P3.1 (TxD) – Serial Output Port (Connected to SERIAL TRANSMIT BUFFER) P3.2 (INT0) – External Level or Edge Triggered General Purpose Interrupt 0. P3.3 (INT1) - External Level or Edge Triggered General Purpose Interrupt 1. P3.4 (T0) – Clock pulse input to TIMER 0 when acting as COUNTER. P3.5 (T1) - Clock pulse input to TIMER 1 when acting as COUNTER. P3.6 (WR ) – Acts as MEMORY WRITE SIGNAL for EXTERNAL RAM. P3.7 (RD) - Acts as MEMORY READ SIGNAL for EXTERNAL RAM or ROM.</td>
</tr>
<tr>
<td>29</td>
<td>PSEN (Program Store Enable)</td>
<td>Acts as MEMORY READ SIGNAL for EXTERNAL ROM.</td>
</tr>
<tr>
<td>Pin</td>
<td>Description</td>
<td>Notes</td>
</tr>
<tr>
<td>-----</td>
<td>-------------</td>
<td>-------</td>
</tr>
<tr>
<td>30</td>
<td><strong>ALE / PROG</strong></td>
<td>Activated every two machine cycle when 8051 executes code from external memory. Serves as ADDRESS LATCH ENABLE SIGNAL for DEMULTIPLEXING AD7-AD0 bus during EXPANDED MODE. Also serves as PROGRAM PULSE INPUT during EPROM PROGRAMMING.</td>
</tr>
<tr>
<td>31</td>
<td><strong>EA/V&lt;sub&gt;PP&lt;/sub&gt;</strong></td>
<td>When low, it indicates 8051 is operating in SINGLE CHIP MODE. In this mode, 8051 access codes from 0000H to 0FFFH from INTERNAL ROM and codes from 1000H to FFFFH from EXTERNAL ROM. When high, it indicates 8051 is operating in EXPANDED MODE. In this mode, 8051 access codes from 0000H to FFFFH from EXTERNAL ROM. Also serves PROGRAMMING SUPPLY VOLTAGE during EEPROM PROGRAMMING.</td>
</tr>
</tbody>
</table>
| 9   | **RESET** | A high on this pin for TWO MACHINE CYCLES WHILE OSCILLATOR IS RUNNING RESETS 8051 MICROCONTROLLER. After a RESET operation following is the status of internal registers:  
- PC initialized to 0000H  
- SP initialized to 07H  
- Register Bank 0 selected |
| 18-19 | **XTAL 1, XTAL 2** | XTAL 1 - Input to the ON-CHIP INVERTING AMPLIFIER  
XTAL 2 – Output from the ON-CHIP INVERTING AMPLIFIER. Quartz crystal or ceramic resonator connected between XTAL 1 and XTAL 2 when ON-CHIP AMPLIFIER functions as ON-CHIP OSCILLATOR.  
External CLOCK SOURCE is connected to XTAL 2. Under this condition, the ON-CHIP AMPLIFIER acts as SIGNAL CONDITIONER. |
3. Port Structure of 8051 Microcontroller

Port 0:

- 8-bit Bidirectional I/O port in SINGLE CHIP MODE.
- Serves as LOWER ORDER MULTIPLEXED ADDRESS and DATA BUS (AD7-AD0) in EXPANDED MODE. Uses INTERNAL PULL-UP RESISTORs in this case.
- Transmits CODE BYTES during program verification of ROM. Uses EXTERNAL PULL-UP RESISTORS in this case.
- When a pin has 1 in it, it acts INPUT PIN. When a pin has 0 in it, it acts as OUTPUT PIN.
- Port 0 is a TRUE BIDIRECTIONAL PORT; Provisions are there for READING the CONTENTS of LATCH and PIN.
- The top and bottom transistors are NMOS transistors. The top input of MUX [Connected to inverter] is labeled as 1 and lower input of MUX[connected to \( Q \) of D-latch) is labeled as 0.
- When CONTROL LINE is 0, the port functions as NORMAL BIDIRECTIONAL I/O port. Under this condition, writing “1” to the LATCH makes the PORT PIN to function as INPUT or OUTPUT port.
- When CONTROL LINE is 1, the port functions as ADDRESS/DATA BUS. Under this condition, writing “1” to the LATCH makes the PORT PIN to function as INPUT PIN and writing “0” to the LATCH makes the PORT PIN to function as OUTPUT PIN.

Port 1:

- 8-bit Bidirectional I/O port in SINGLE CHIP MODE and EXPANDED mode.
- Receives A0-A7 during program verification of ROM.
- When a pin has 1 in it, it acts INPUT PIN. When a pin has 0 in it, it acts as OUTPUT PIN.
- Has Internal PULL-UP RESISTORS.
- Port 1 is a QUASI-BIDIRECTIONAL PORT.
- Writing “1” to the latch makes the PORT PIN to function as INPUT PORT. Writing “0” to the latch makes the PORT PIN to function as OUTPUT PORT.

**Port 2:**

![Port 2 Diagram]

Structure of Port 2 pin.
- 8-bit Bidirectional I/O port in SINGLE CHIP MODE.
- Serves as HIGHER ORDER ADDRESS BUS (A15-A8) in EXPANDED MODE.
- When a pin has 1 in it, it acts INPUT PIN. When a pin has 0 in it, it acts as OUTPUT PIN.
- When CONTROL LINE is 0, the port functions as NORMAL BIDIRECTIONAL I/O port. Under this condition, writing “1” to the LATCH makes the PORT PIN to function as INPUT or OUTPUT port. Here an NMOS transistor functions as PULL-UP RESISTOR.
- When CONTROL LINE is 1, the port functions as ADDRESS BUS. Under this condition, writing “1” to the LATCH makes the PORT PIN to function as INPUT PIN and writing “0” to the LATCH makes the PORT PIN to function as OUTPUT PIN.

**Port 3:**

![Port 3 Diagram]

Structure of Port 3 pin.
- 8-bit Bidirectional I/O port in SINGLE CHIP MODE. Has Internal PULL-UP RESISTORS.
- Special purpose I/O pins in EXPANDED MODE.
- P3.0 (RxD) – Serial Input Port (Connected to SERIAL RECEIVE BUFFER)
- P3.1 (TxD) – Serial Output Port (Connected to SERIAL TRANSMIT BUFFER)
- P3.2 (INT0) – External Level or Edge Triggered General Purpose Interrupt 0.
- P3.3 (INT1) - External Level or Edge Triggered General Purpose Interrupt 1.
- P3.4 (T0) – Clock pulse input to TIMER 0 when acting as COUNTER.
- P3.5 (T1) - Clock pulse input to TIMER 1 when acting as COUNTER.
- P3.6 (WR) – Acts as MEMORY WRITE SIGNAL for EXTERNAL RAM.
- P3.7 (RD) - Acts as MEMORY READ SIGNAL for EXTERNAL RAM.
- Writing “1” to the LATCH makes the PORT pin to function as INPUT PIN. Writing “0” to the LATCH makes the PORT pin to function as OUTPUT pin.

4. Operating Modes of Serial Communication in 8051 Microcontroller

Mode 0:
- 8-bits are TRANSMITTED and RECEIVED through RxD(Receive Data) pin.
- TxD(Transmit Data) pin acts as the shifting clock.
- Baud Rate is fixed and is given by \[ \frac{\text{Oscillator Frequency}}{12} \]

Mode 1:
- 10-bits are transmitted through TxD pin and received through RxD pin.
- Composition of 10-bits = Start bit (0) + 8-data bits (Least significant bit transmitted or received first)+ Stop bit(1).
- On receive, stop bit goes into RB 8 bit of SCON register
- Baud rate is variable and is given by \[ \frac{K \times \text{Oscillator Frequency}}{32 \times 12 \times (256 - TH1)} \]; If SMOD = 0, then K = 1 and if SMOD = 1, then K = 2. This equation holds, provided TIMER 1 operates in MODE 2. If TIMER 1 is operated in other modes, the baud rate is given as follows:
- \[ 2^{32} \times \text{Timer 1 overflow frequency} \]

<table>
<thead>
<tr>
<th>Value of TH1 in Hexadecimal format</th>
<th>Baud rate (SMOD = 0)</th>
<th>Baud Rate (SMOD = 1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>FD_H</td>
<td>9600</td>
<td>19,200</td>
</tr>
<tr>
<td>FA_H</td>
<td>4800</td>
<td>9600</td>
</tr>
<tr>
<td>F4_H</td>
<td>2400</td>
<td>4800</td>
</tr>
<tr>
<td>E8_H</td>
<td>1200</td>
<td>2400</td>
</tr>
</tbody>
</table>

Assumed Crystal Input Frequency = 11.0592 MHz

Mode 2:
- 11-bits are transmitted through TxD pin or received through RxD pin.
- Composition of 11-bits = Start bit (0) + 8-data bits (Least significant bit transmitted or received first) + Programmable 9th bit + Stop bit (1)
- On Transmit, programmable 9th bit goes into TB 8 bit of SCON register
- On Receive, programmable 9th bit goes into RB 8 bit of SCON register; Stop bit is ignored.
- Baud rate is fixed and is given by \[ \frac{\text{Oscillator Frequency}}{32} \] for SMOD = 1 [Baud Rate is doubled]
- \[ \frac{\text{Oscillator Frequency}}{64} \] for SMOD = 0
Mode 3:

- 11-bits are transmitted through TxD pin or received through RxD pin.
- Composition of 11-bits = Start bit (0) + 8-data bits (Least significant bit transmitted or received first) + Programmable 9\textsuperscript{th} bit + Stop bit (1)
- On Transmit, programmable 9\textsuperscript{th} bit goes into TB 8 bit of SCON register
- On Receive, programmable 9\textsuperscript{th} bit goes into RB 8 bit of SCON register; Stop bit is ignored.

Baud rate is variable and is given by \[ K \times \frac{\text{Oscillator Frequency}}{32 \times 12 \times (256 - TH1)} \]; If SMOD = 0, then K = 1 and if SMOD = 1, then K = 2. This equation holds, provided TIMER 1 operates in MODE 2. If TIMER 1 is operated in other modes the baud rate is given as follows:

\[ \frac{2^{32}\times \text{Timer 1 overflow frequency}}{32} \]

<table>
<thead>
<tr>
<th>Value of TH1 in Hexadecimal format</th>
<th>Baud rate (SMOD = 0)</th>
<th>Baud Rate (SMOD = 1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>FD\textsubscript{H}</td>
<td>9600</td>
<td>19,200</td>
</tr>
<tr>
<td>FA\textsubscript{H}</td>
<td>4800</td>
<td>9600</td>
</tr>
<tr>
<td>F4\textsubscript{H}</td>
<td>2400</td>
<td>4800</td>
</tr>
<tr>
<td>E8\textsubscript{H}</td>
<td>1200</td>
<td>2400</td>
</tr>
</tbody>
</table>

Assumed Crystal Input Frequency = 11.0592 MHz

Special Purpose Registers associated with Serial Communication:

**SCON [Serial Communication CONtrol] Register**:

<table>
<thead>
<tr>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SM0</td>
<td>SM1</td>
<td>SM2</td>
<td>REN</td>
<td>TB 8</td>
<td>RB 8</td>
<td>TI</td>
<td>RI</td>
</tr>
</tbody>
</table>

**SM 2 = 1**, Frames that are not having programmable 9\textsuperscript{th} bit are not received.

REN = 1, Data Reception Enabled
TB 8 = 1, 9\textsuperscript{th} bit transmitted during MODE 2 and 3
RB 8 = 1, 9\textsuperscript{th} bit Received during MODE 2 and 3
TI [Transmit Interrupt ] = 1, Completed transmission of 8-data bits.
RI [Received Interrupt ] = 1, Completed reception of 8-data bits.

**PCON [Power Mode CONtrol] Register**:

<table>
<thead>
<tr>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SMOD</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>GF1</td>
<td>GF0</td>
<td>PD</td>
</tr>
</tbody>
</table>

SMOD [Serial Baud Rate Modifier] bit = 1, Baud Rate Doubled
GF1, GF0 – General Purpose User Programmable Flags [Indicates whether an interrupt occurred during Normal Mode or Idle Mode]
PD [Power Down] = 1, Oscillator Turned OFF.
IDL [Idle Mode] = 1, CPU Turned OFF.
5. Operating Modes of Timer/Counter in 8051 Microcontroller

Mode 0: (13-bit TIMER/COUNTER MODE)

- Mode 1 is also applicable to Timer 1, in which case it is split into TL1 and TH1 bits.
- When operating as a timer, Internal Oscillator provides the clocking pulse via divide-by-12 counter.
- When operating as a counter, T0 or T1 pin provides the clocking pulse.
- The lower order byte of Timer 0 or Timer 1 in Timer or Counter, divides the clock pulse frequency further by 5.
- The Timer 0 or Timer 1 acts a SYNCHRONOUS UP-COUNTER both in TIMER or COUNTER MODE and counts from 0000H to 1FFFH.
- When Timer 0 or Timer 1 overflow occurs in TIMER or COUNTER MODE, the TIMER or COUNTER OVERFLOW FLAG is set, which acts as one of the HARDWARE INTERRUPTs. Overflow is the process where the counter or timer is reinitialized to its beginning count after reaching its terminal count.

Mode 1: (16-bit TIMER/COUNTER MODE)

- Mode 1 is also applicable to Timer 1, in which case it is split into TL1 and TH1 bits.
- When operating as a timer, Internal Oscillator provides the clocking pulse via divide-by-12 counter.
- When operating as a counter, T0 or T1 pin provides the clocking pulse.
- The lower order byte of Timer 0 or Timer 1 in Timer or Counter, divides the clock pulse frequency further by 8.
- The Timer 0 or Timer 1 acts a SYNCHRONOUS UP-COUNTER both in TIMER or COUNTER MODE and counts from 0000H to FFFFH.
- When Timer 0 or Timer 1 overflow occurs in TIMER or COUNTER MODE, the TIMER or COUNTER OVERFLOW FLAG is set, which acts as one of the HARDWARE INTERRUPTs. Overflow is the process where the counter or timer is reinitialized to its beginning count after reaching its terminal count.
Mode 2: (8-bit Timer/Counter with auto-reload)

Mode 2 – 8 bit operation with auto reload

- Mode 2 is also applicable to Timer 1, in which case it is split into TL1 and TH1 bits.
- When operating as a timer, Internal Oscillator provides the clocking pulse via divide-by-12 counter.
- When operating as a counter, T0 or T1 pin provides the clocking pulse.
- The HIGHER order byte of Timer 0 or Timer 1 in Timer or Counter, stores the count value to be initialized into LOWER ORDER BYTE of TIMER 0 or TIMER 1 once it has completed counting. The Timer 0 or Timer 1 acts a SYNCHRONOUS UP-COUNTER both in TIMER or COUNTER MODE and counts from 00H to FFH.
- When Timer 0 or Timer 1 overflow occurs in TIMER or COUNTER MODE, the TIMER or COUNTER OVERFLOW FLAG is set, which acts as one of the HARDWARE INTERRUPTS. Overflow is the process where the counter or timer is reinitialized to its beginning count after reaching its terminal count.
Mode 3: (8-bit Timer/Counter without auto-reload)

**Mode 3 – Split operation – Timer 0**

- Mode 3 is equally applicable to TIMER 1, in which case it is split into TH1 and TL1 bits.
- In this mode, the LOWER ORDER and HIGHER ORDER BYTES of Timer 0 or Timer 1, acts as INDIVIDUAL TIMER or COUNTER.
- The lower order byte can be either run from INTERNAL OSCILLATOR or external T0 / T1 pin.
- The higher order byte is entirely run from internal oscillator.
- The LOWER ORDER and HIGHER ORDER BYTE of Timer 0 or Timer 1 acts a SYNCHRONOUS UP-COUNTER both in TIMER or COUNTER MODE and counts from 00H to FFH.
- When Timer 0 or Timer 1 overflow occurs in TIMER or COUNTER MODE, the TIMER or COUNTER OVERFLOW FLAG is set, which acts as one of the HARDWARE INTERRUPTS. Overflow is the process where the counter or timer is reinitialized to its beginning count after reaching its terminal count.

- The HARDWARE way of CONTROLLING the START and STOP of TIMER/COUNTER is through setting and resetting of GATE signal. When GATE signal is activated [logic 1 placed in GATE signal], INT 0 or INT 1 pins AND TR 0 / TR 1 BITS controls the START and STOP of TIMER/COUNTER. When GATE signal is deactivated [logic 0 placed in GATE signal], SOFTWARE CONTROLS the START and STOP of TIMER 0 and TIMER 1 through TR 0 / TR 1 bits.

SFRs associated with TIMER/COUNTER MODULE of 8051 Microcontroller

**TMOD** (TIMER/COUNTER OPERATING MODE SELECTION) register:

<table>
<thead>
<tr>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>GATE</td>
<td>C/T*</td>
<td>M1</td>
<td>M0</td>
<td>GATE</td>
<td>C/T*</td>
<td>M1</td>
<td>M0</td>
</tr>
</tbody>
</table>

**TIMER/COUNTER 1**

- GATE = 1, INT 0 / INT 1 pins control the START and STOP of TIMER/COUNTER 0 or 1.
- C/T* = 1, TIMER/COUNTER MODULE acts as COUNTER; C/T* = 0, TIMER/COUNTER MODULE acts as TIMER

**Operating Modes**

<table>
<thead>
<tr>
<th>M1</th>
<th>M0</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>13-bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TIMER/COUNTER</td>
</tr>
<tr>
<td>D7</td>
<td>D6</td>
<td>D5</td>
</tr>
<tr>
<td>----</td>
<td>----</td>
<td>----</td>
</tr>
<tr>
<td>TF1</td>
<td>TR1</td>
<td>TF0</td>
</tr>
</tbody>
</table>

TF0 / TF1 = 1, TIMER/COUNTER 0 or 1 OVERFLOW OCCURRED
TR0 / TR1 = 1, ENABLED for HARDWARE and SOFTWARE CONTROL of START of TIMERS/COUNTERS.
IE0 / IE1 = 1, ENABLED to indicate a NEGATIVE EDGE has occurred in INT 0 and INT 1 pins.
IT0 / IT1 = 1, ENABLED to indicate a NEGATIVE LEVEL has occurred in INT 0 and INT 1 pins.

6. Interrupt Structure of 8051 Microcontroller

- 8051 provides 5 hardware vectored interrupt sources
- The interrupt sources are: TWO LEVEL or EDGE TRIGGERED GENERAL PURPOSE INTERRUPTS (INT0, INT1), TWO TIMER/COUNTER OVERFLOW INDICATION INTERRUPTS (TF1, TF0), ONE SERIAL COMMUNICATION COMPLETE INDICATION INTERRUPT (RI + TI).
- Two SFRs associated with INTERRUPT STRUCTURE of 8051 Microcontroller are:
  INTERRUPT ENABLE (IE):

EA = 1, Each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
= 0, No interrupt will be acknowledged.

ES = 1, Serial Communication Completion Interrupt Recognized.
ET1/ET0 = 1, Timer/Counter 1 or 0 Overflow Indication Interrupt Recognized.
EX1/EX0 = 1, External Level or Triggered Interrupt 1 or 0 Recognized.

**INTERRUPT PRIORITY (IP):**

<table>
<thead>
<tr>
<th>PS</th>
<th>PT1</th>
<th>PT0</th>
<th>PX1</th>
<th>PX0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

- A low priority interrupt can be INTERRUPTED by a higher priority interrupt, but not by another lower priority interrupt; A high priority interrupt can't be interrupted by any other interrupt source.

- **8051 supports two priority levels:**
  If two interrupt requests of same priority levels are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level, there is a second priority structure determined by polling sequence.

- All the interrupt flags are latched onto the interrupt control system during State 5 of every machine cycle. If the flag of an enabled interrupt is found to be set, the interrupt control system generates an LCALL(Long CALL) to the appropriate location in Program Memory. A minimum of three complete machine cycles elapse between the activation of external interrupt request and beginning of the execution of first instruction of service routine.

- In case of serial communication completion interrupt, it is the work of the INTERRUPT SERVICE ROUTINE to determine, whether it is because of TRANSMISSION COMPLETE or RECEPTION COMPLETE.

<table>
<thead>
<tr>
<th>Source</th>
<th>Vector Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>IE0</td>
<td>0003H</td>
</tr>
<tr>
<td>TF0</td>
<td>000BH</td>
</tr>
<tr>
<td>IE1</td>
<td>0013H</td>
</tr>
<tr>
<td>TF1</td>
<td>001BH</td>
</tr>
<tr>
<td>RI + TI</td>
<td>0023H</td>
</tr>
</tbody>
</table>

- In case of EXTERNAL GENERAL PURPOSE INTERRUPT is LEVEL TRIGGERED, the on-chip INTERRUPT CONTROL SYSTEM clears the corresponding INTERRUPT request flag. In case of EXTERNAL GENERAL PURPOSE INTERRUPT is EDGE TRIGGERED, the external requesting source clears the CORRESPONDING INTERRUPT REQUEST FLAG. In case of EXTERNAL GENERAL PURPOSE INTERRUPT is LEVEL TRIGGERED, it must be held high or low for atleast one machine cycle to get recognized by on-chip INTERRUPT CONTROL SYSTEM. In case of EXTERNAL GENERAL PURPOSE INTERRUPT is EDGE TRIGGERED, it must be held HIGH for atleast ONE MACHINE CYCLE and low for atleast ONE MACHINE CYCLE to get recognized by on-chip INTERRUPT CONTROL SYSTEM.
7. Memory Organization of 8051 Microcontroller

Structure of On-CHIP RAM or DATA MEMORY of 8051 microcontroller:

- 8051 has 256 bytes of internal RAM or on-chip RAM
- The 256 bytes locations are split into two: Lower 128 bytes location + Upper 128 bytes location.
- The lower 128 bytes location are split-up as follows:
  - First 32 bytes from locations 00H to 1FH constitute WORKING REGISTERS or REGISTER BANK; There are totally 4 register banks namely BANK 0, BANK 1, BANK 2, BANK 3; Each BANK consist of 8 8-bit Registers. Each register can be accessed by its name or RAM address; Only one register bank can be used at a time; The register banks that are not in use can be used as GENERAL PURPOSE RAM; On reset, BANK 0 is selected as DEFAULT REGISTER BANK.
  - Next 16 bytes from locations 20H to 2FH constitute BIT ADDRESSABLE AREA. In this portion, each bit of memory location has an address allocated to it and can be set by “SETB bit” instruction and reset or cleared by “CLR bit or CPL bit” instruction.
  - Last 80 bytes from locations 30H to 7FH constitute GENERAL PURPOSE area.
  - The first 32 bytes and last 80 bytes of RAM locations are BYTE ADDRESSABLE. Each memory location can be accessed as a whole 8-bit and not individual bits.
- The upper 128 bytes of location are filled with SPECIAL FUNCTION REGISTERS or SPECIAL PURPOSE REGISTERS. They contain registers for controlling the ALU, ON-CHIP PERIPHERALS, PORTS.
The Register banks are selected by setting RS1 and RS0 bits of PSW to appropriate values:

<table>
<thead>
<tr>
<th>RS1</th>
<th>RS0</th>
<th>Register Bank</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Select register bank 0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Select register bank 1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Select register bank 2</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Select register bank 3</td>
</tr>
</tbody>
</table>

**Accessing External Data Memory:**
- Port 0 serves as lower order multiplexed address and data bus (AD7 – AD0).
- Three lines of PORT 2 are being used to PAGE the RAM.
- The CPU generates RD and WR signals needed during EXTERNAL RAM access.
- The external DATA memory can have 64KB of memory locations.
- External Data memory addresses can be 1-byte or 2-byte wide.
- The following diagram shows hardware configuration for accessing 2K bytes of external RAM.

**Structure of ON-CHIP ROM or PROGRAM MEMORY:**
- After reset, CPU begins execution from on-chip program memory location 0000H.
• The vector addresses for the 5 hardware interrupts are assigned 8 memory locations each in the on-chip program memory.
• In the 4KB ROM based 8051 microcontroller, if EA pin is strapped to Vcc, then program fetches to address 0000H to 0FFFH are directed to internal ROM and program fetches to address 1000H to FFFFH are directed to external ROM.
• If EA pin is strapped to Vss, then program fetches to address 0000H to FFFFH are directed to external ROM.
• The read strobe to external ROM, PSEN, is used for all external program fetches. PSEN is not activated for internal program fetches.

**Accessing EXTERNAL ROM:**

• Port 0 serves as LOWER ORDER MULTIPLEXED ADDRESS/DATA BUS (AD7-AD0). It emits lower byte of PC(PCL) as address. During this time, it is latched by the ALE signal.
• Port 2 emits the HIGHER ORDER ADDRESS BUS. Then PSEN enables the EXTERNAL ROM and the code byte is read into the microcontroller from the addressed location.
• Program memory addresses are always 16-bits wide, even though program memory capacity is less than 64KB.