R.M.D. ENGINEERING COLLEGE

DEPARTMENT OF INFORMATION TECHNOLOGY

CS8351 – DIGITAL PRINCIPLES AND SYSTEM DESIGN

REGULATION – 2017

II YEAR/III SEMESTER

PART-B AND PART-C POSSIBLE QUESTIONS

UNIT-I

1. Express the following function in the sum of min terms and product of max terms :

   (AB+C)(B+C'D) (b) x'+x(x+y')(y+z')

2. Subtract 748 from 963 using 10's complement

3. Find (22)10-(11)10 using 9's complement

4. Simplify the following Boolean expression in SOP and POS using KMAP

   AC' +B'D+A'CD+ABCD

5. Simplify the function F(w,x,y,z)=∑(2,3,12,13,14,15) using map method and implement using NAND gates.

6. Simplify the following functions using K-Map technique and implement using NOR gates

   F(W,X,Y,Z)=∑m(0,6,8,13,14)+∑d(2,4,10)

10. Simplify the Boolean **Function F = Σ (0, 1, 2, 3, 8, 9, 16, 17, 20, 21, 24, 25, 28, 29, 30, 31)** using K-map

11. Express the following function in the sum of min terms and product of max terms

    F(x,y,z)=x+yz

12. Find the following function as a sum of min terms and product of max terms
    F(A,B,C) =BD'+AD+BD

13. Reduce the following Boolean expressions

    a) A'C' +ABC+AC'+AB' b) x'yz+xz+x'z

14. Simplify the following Boolean expression to minimum number of literals

    a) (x+y+z) (x'+y'+z) (b) (A+B)' (A'+B')'

15. (i) Perform subtraction using 2's complement 1010100 – 1000011

    (ii)Perform subtraction using 1's complement 1010100-1000011

(iii)Perform subtraction using 10's complement 125-1800

(iv)Perform subtraction using 9's complement 125-1800

16. (i)Find $(11)_{10} - (22)_{10}$ using 10's complement.

    (ii)Show that excess-3 code is a self-complementing code

17. (i) Subtract 748 from 963 using 10's complement

    (ii)Find $(22)_{10}$-$(11)_{10}$ using 9's complement

18. (i)Perform the following decimal addition $(589)_{10} + (199)_{10}$ in BCD

    (ii)Write a short note on (a) Error detecting codes (b) ASCII codes

19. (i) Perform $(51)_{10} - (37)_{10}$ using 1's and 2's complement.

    (ii) Write a short note on (a)Gray code (b) Excess-3 code

20. Simplify the following functions using K-Map technique
    (i) $G=\pi (0,3,7,9,11)$
    (ii) $F(W,X,Y,Z)=\sum m(0,7,8,9,10,12)+\sum d(2,5,13)$

21. i.Simplify the Boolean function in SOP and POS $F(A,B,C,D)=\sum m(0,1,2,5,8,9,10)$
    ii. Plot the following Boolean function in K Map and simplify it.
    $F(w,x,y,z)=\sum m(0,1,2,4,5,6,8,9,12,13,14)$

22. Simplify the following Boolean expression in SOP and POS using KMAP
    AC' +B'D+A'CD+ABCD

23. Simplify the following Boolean expression using four variable maps

    xyz+wy+wxy'+x'y

24. Simplify the Boolean function using map method

    $F(w,x,y,z)=\sum(0,2,4,6,8,10,12,14)$

25. Simplify the following functions using K-Map technique
    $F(W,X,Y,Z)=\sum m(0,7,8,9,10,12)+\sum d(2,5,13)$

26. Simplify the following functions using K-Map technique
    $F(W,X,Y,Z)=\sum m(0,6,8,13,14)+\sum d(2,4,10)$

27. Simplify the Boolean function F= x'z+ w'xy'+ w(x'y+xy')

28. Simplify the following functions using K-Map technique
    $F(W,X,Y,Z)=\sum m(1,3,8,13,14)+\sum d(2,4,10)$

UNIT – II

1. Design a combinational circuit that converts 8421 BCD code to Excess-3 code.
2. With a neat diagram explain half adder.
3. Design and construct a 4-bit magnitude comparator.
4. Explain encoder in detail.
5. With suitable block diagram explain binary multiplier.
6. Write a detailed note on carry propagation.
7. Explain HDL models for combinational circuits.
8. Implement a full adder with two 4x1 Multiplexers.
9. Design and implement an 8421 to gray code converter. Realize the converter using only NAND gates.
10. Explain and design a half adder and full adder circuit.
11. Explain and design half subtractor and full subtractor circuit.
12. Design and explain a 3 to 8 line decoder using combinational circuits.
13. Explain a 2 X 4 decoder and construct it using NAND gate.
14. Implement the following Boolean function using 8:1 MUX.
    i) $F(P,Q,R,S) = \sum m(0,1,3,4,8,9,15)$
    ii) $F(A,B,C,D) = \prod M(0,3,5,8,9,10,12,14)$
15. Explain De-multiplexer with a logic diagram
16. Implement a De-multiplexer using Decoder with Enable.
17. Design 1:8 De-multiplexer using two 1:4 De-multiplexers.
18. i) Implement the following Boolean function with 8:1 MUX.
    $F(A,B,C,D) = \sum m(0,2,6,10,11,12,13)$
    ii) Implement the following Boolean function with 8:1 MUX.
    $F(A,B,C,D) = A'BD' + ACD + B'CD + A'C'D$
19. Design a combinational logic circuit whose outputs are
    $F1 = a'bc + ab'c$ and $F2 = a' + b'c + bc'$
20. i) Design a combinational logic circuit with three input variables that will produce a logic high output when more than one input variables are logic low.
    ii) Discuss the procedure to design a combinational circuit.
21. Explain gate level modeling and data flow modeling in HDL.

UNIT – III

1. Design SR latch using NAND and NOR gate.

2. How the race condition can be avoided in a flip flop.

3. With neat diagram, explain about JK flip flop.

4. Draw T flip flop using logic gates and explain its working.

5. Write about SR and D latch with a neat diagram and explain its working.

6. Implement JK flip flop using D flip flop.

7. State the procedure for designing Synchronous sequential circuits.

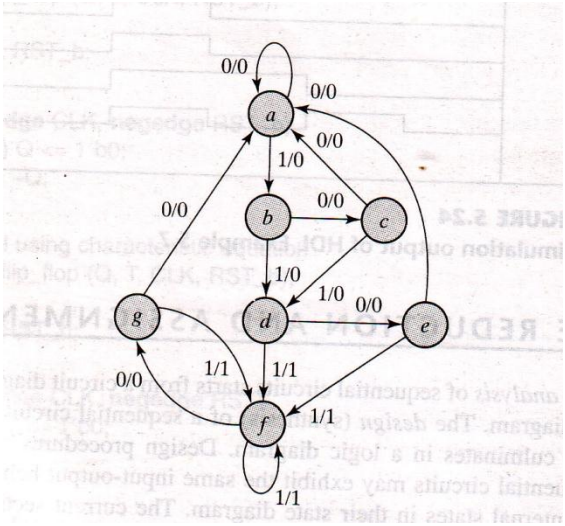
8. A sequential circuit with two D Flip-flops A and B, one input x , and one output z is specified by the following next state and output equations: A(t+1) = A'+B; B(t+1)=B'x ; z =A+B'
   (i)Draw the logic diagram of the circuit.
   (ii)Derive the state table.
   (iii)Draw the state diagram of the circuit.

9. Explain the difference between a state table, characteristic table and an excitation table.

10. A sequential circuit with two D Flip-flops A and B, one input x , and one output y is specified by the following next state and output equations: A(t+1) = Ax+ Bx ; B(t+1)=A'x ; y =(A+B) x'
   (i)Draw the logic diagram of the circuit.
   (ii)Derive the state table.
   (iii)Draw the state diagram of the circuit.

11. Design a sequence detector that detects a sequence of three or more consecutive 1's in a string of bits coming through an input line and produces an output whenever this sequence is detected.

12. Implement state reduction and state assignment for the following state diagram.



13. Explain shift register and design a serial in serial out shift register.

14. Explain the different types of shift registers with a neat diagram.

15. Explain how shift registers are used in serial addition with a neat diagram..

16. Design a 4 bit shift register using JK flip flop.

17. Design a 4 bit shift register using D flip flop.

18. Design a Mod-10 synchronous counter using JK flip flops. Write excitation table and state table.

19. Design a synchronous counter using JK flip flop to count the following sequence 7,4,3,1,5,0

20. Design a 4 bit BCD counter that counts in the following way : 0000,0001,……,1001 and back to 0000.

21. Design a Binary counter using T flip flops to counts in the following sequence:
000,001,010,011,100,101,111,000

22. Design a Modulo-5 synchronous counter using JK flip flop and implement it.

23. Explain the data flow HDL model for shift registers.

24. Explain the behavior HDL model for 4-bit binary synchronous counter.

25. A sequential circuit with two D flip-flops A and B, two inputs, x and y ; and one output z is specified by the following next-state and output equations

$A(t + 1) = xy'+xB$

$B(t + 1) = xA+xB'$

$Y = A$

(a) Draw the logic diagram of the circuit.

(b) List the state table for the sequential circuit.

(c) Draw the corresponding state diagram.

26. A sequential circuit has two JK flip-flops A and B and one input x . The circuit is described by the following flip-flop input equations:

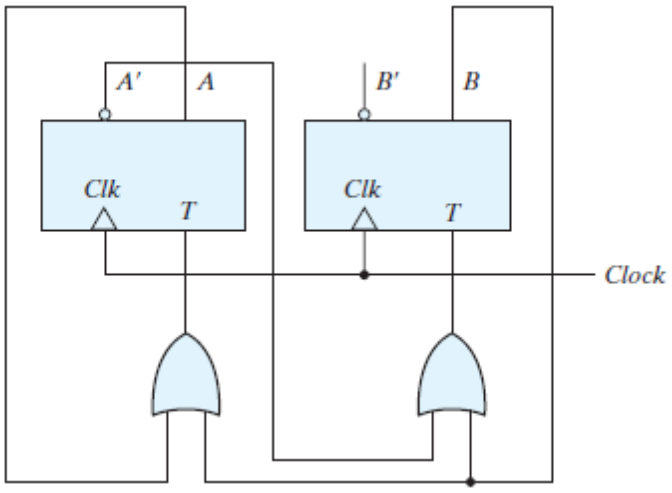
$J_A = x \quad K_A = B$

$J_B = x \quad K_B = x$

(a) Derive the state equations A (t + 1) and B (t + 1) by substituting the input equations for the J and K variables.

(b) Draw the state diagram of the circuit.

27. Derive the state table and the state diagram of the sequential circuit shown in the following diagram. Explain the function that the circuit performs.



28. A sequential circuit has two JK flip-flops A and B, two inputs x and y, and one output z .

The flip-flop input equations and circuit output equation are

$J_A = Bx + B'y'$ $K_A = B'xy'$

$J_B = A'x$ $K_B = A + xy'$

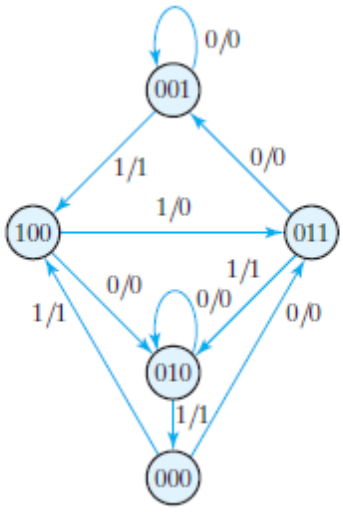
$z = Ax'y' + Bx'y'$

(a) Draw the logic diagram of the circuit.

(b) Tabulate the state table.

(c) Derive the state equations for A and B .

29. Design a sequential circuit specified by the following state diagram using T flip flop



30. For the following state table

Present State	Next State		Output	
	X = 0	X = 1	X = 0	X = 1
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

(a) Draw the corresponding state diagram.

(b) Tabulate the reduced state table.

(c) Draw the state diagram corresponding to the reduced state table.

31. Design a counter with the following repeated binary sequence: 0, 2, 4, 6, 8.

32. Design a four-bit binary synchronous counter with D flip-flops.

33. Design a 4-bit BCD ripple counter.

UNIT – IV

1. An asynchronous sequential circuit is described by the following excitation and output function.
   $Y=X_1X_2+(X_2+X_3)y$ and $z=y$
   i. Draw the logic diagram of the circuit.
   ii. Derive the transition table and output map.
   iii. Describe the behavior of the circuit.

2. Analyze the asynchronous sequential circuit described by the following excitation and output function.

   Y=X1X2+(X2+X3)y and z=y. Give the logic diagram, transition table and output map.

3. Analyze the asynchronous sequential circuit described by the following excitation function.

   Y1 = xy1 + x'y2 ; Y2 = xy1' + x'y2. Give the logic diagram, transition table and output map.

4. Draw the logic diagram and derive the transition table and output map for the circuit with the given excitation and output function. $Y=X_1X_2+(X_2+X_3)y$ and $z=y$.

5. Explain critical races and non-critical races with examples?

6. What is the purpose of a merger diagram? Explain with an example.

7. How critical race and non-critical race conditions can be detected and avoided in an asynchronous sequential circuit.

8. What is an implication table? Draw the implication table for the given state table and draw the reduced state table.

Present state	Next state		Output	
	x = 0	x=1	x = 0	x=1
a	d	b	0	0
b	e	a	0	0
c	g	f	0	1
d	a	d	1	0
e	a	d	1	0
f	c	b	0	0
g	a	e	1	0

9. Give a race free state assignment for the reduced flow table shown.

	00	01	11	10
a	b	(a)	d	(a)
b	(b)	d	(b)	a
c	(c)	a	b	(c)
d	c	(d)	(d)	c

10. What is a Hazard? Explain the types? Check whether the following circuit contains a hazard or not $Y = x_1x_2 + x_2'x_3$ If the hazard is present, demonstrate its removal.

11. What are Essential hazards and find a Static and Dynamic free realization for the following function using NAND and NOR gates. $F(a,b,c,d)= \Sigma m(1,5,7,14,15)$.

12. Discuss about static, dynamic and essential hazards in asynchronous sequential circuits.

13. Implement the switching function $F=\Sigma m(1,3,5,7,8,9,14,15)$ by a static hazard free two level AND-OR gate network

14. Explain the steps in the design of asynchronous sequential circuits with an example.

UNIT – V

1. Tabulate the PLA programming table for the four Boolean functions listed below. Minimize the numbers of product terms.

   $A(x, y, z) = \sum(1, 3, 5, 6)$

   $B(x, y, z) = \sum (0, 1, 6, 7)$

   $C(x, y, z) = \sum (3, 5)$

   $D(x, y, z) = \sum (1, 2, 4, 5, 7)$

2. Tabulate the truth table for an 8 * 4 ROM that implements the Boolean functions

   $A(x, y, z) = \sum (0, 3, 4, 6)$

   $B(x, y, z) = \sum (0, 1, 4, 7)$

   $C(x, y, z) = \sum (1, 5)$

   $D(x, y, z) = \sum (0, 1, 3, 5, 7)$

3. Derive the PLA programming table for the combinational circuit that squares a three-bit number. Minimize the number of product terms.

4. Derive the ROM programming table for the combinational circuit that squares a 4-bit number. Minimize the number of product terms.

5. Draw a PLA circuit to implement the functions

   F1 = A'B + AC + A'BC'

   F2 = (AC + AB + BC)'

6. Implement the following two Boolean functions with a PLA:

   $F1(A, B, C) = \sum (0, 1, 2, 4)$

   $F2(A, B, C) = \sum (0, 5, 6, 7)$

7. Implement the following four Boolean functions with a PAL

   w(A, B, C, D) = g(2, 12, 13)

   x(A, B, C, D) = g(7, 8, 9, 10, 11, 12, 13, 14, 15)

   y(A, B, C, D) = g(0, 2, 3, 4, 5, 6, 7, 8, 10, 11, 15)

   z(A, B, C, D) = g(1, 2, 8, 12, 13)

8. Implement the following function using PLA

A(x,y,z)= Σm(1,2,4,6)

B(x,y,z)= Σm(0,1,6,7)

C(x,y,z)= Σm(,2,6)

9. Design a combinational circuit using a PROM. The circuit accepts a three bit number and output an excess-3 code.

10. Design a combinational circuit using a ROM. The circuit accepts a three bit number and output a binary number equal to the square of the input number.

11. The following messages have been coded in the even parity Hamming code and transmitted through a noisy channel. Decode the messages, assuming that at most a single error has occurred in each code word.
    (i) 1001001
    (ii) 0111001
    (iii) 1110110
    (iv) 0011011

12. (i) Write short notes on ASIC.
    (ii)Briefly discuss the sequential programmable devices.

13. Implement the following function using PAL

    W(A,B,C,D)= Σm(2,12,13)

    X(A,B,C,D)= Σm(7,8,9,10,11,12,13,14,15)

    Y(A,B,C,D)= Σm(0,2,3,4,5,6,7,8,10,11,15)

    Z(A,B,C,D)= Σm(1,2,8,12,13)

14. Implement the following function using PAL

    A(w,x,y,z)= Σm(2,12,13)

    B(w,x,y,z)= Σm(7,8,9,10,11,12,13,14,15)

    C(w,x,y,z)= Σm(0,2,3,4,5,6,7,8,10,11,15)

    D(w,x,y,z)= Σm(1,2,8,12,13)

15. A 12-bit Hamming code word containing 8 bits of data and 4 parity bits is read from memory. What was the original 8-bit data word that was written into memory if the 12-bit word read out is as follows:

(a) 000011101010 (b) 101110000110 (c) 101111110100